

REMARKS

1. 35 U.S.C. § 112. Rejections.

The Office Action states that "Claims 23-26, and 106-111 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention".

1a. Regarding Claim 23, the Office Action states that "In claim 23, line 2, "a electrically insulative..." is incorrect. It should be --an insulative--."

10 Applicant has amended Claim 23, to claim an interposer, comprising:
an electrically insulative support substrate having a first surface and a second surface;
and
at least one stress metal spring extending at least from the first surface to the second surface of the support substrate, each of the at least one stress metal spring comprising a plurality of metal layers, at least two of the metal layers having different levels of stress, each of the at least one stress metal spring defining a loop structure which is rotated by an effective rotation angle away from the first surface of the support substrate.

20 Support is seen in the Application as filed, at least on page 39, line 24 to page 41, line 9; on page 43, line 30 to page 44, line 30, in Figure 22 to Figure 27; in Figure 39 to Figure 40.

1b. Regarding Claim 106, the Office Action states that "In claim 106, line 2, change "an" to -
-a--between "having" and "a first surface".

25 Applicant has amended Claim 106, to claim a process, comprising the steps of:
providing a compliant carrier having a first surface and a second surface;
adhesively attaching a wafer comprising at least one integrated circuit device lower surface and an upper surface on the first surface of the compliant carrier, each of the at least 30 one integrated circuit having a plurality of electrical connections on the upper surface;
separating each of the at least one integrated circuit devices from the other of the at least one integrated circuit devices;
providing a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

creating a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board.

5 Support is seen in the Application as filed, at least on page 35, line 26 to page 39, line 22; on page 46, line 32 to page 51, line 18; on page 54, line 15 to page 55, line 13, in Figure 18 to Figure 21; in Figure 55 to Figure 59; and in Figure 68 to Figure 71.

10 Applicant therefore respectfully submits that Claim 23 and Claim 106, as amended, overcome the rejections under 35 U.S.C. § 112, and are fully supported by the Application as filed. As dependent claims 24-26 depend from amended Claim 23, and as dependent claims 107-111 depend from amended Claim 106, and inherently contain all the limitations of the claims they depend from, they are seen to overcome the rejections under 35 U.S.C. § 112 as well.

15 2. Claims 21 and 86 are rejected under U.S.C. 102(b) as being anticipated by Fogal et al. (U.S. 5,905,305)

20 Applicant has canceled Claims 21 and 86, without prejudice. Applicant reserves the right to present claims in a subsequent Application.

3-4. Allowable Subject Matter.

25 3. The Office Action states that Claims 22, 87-105 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3a. Applicant has amended Claim 22 to claim an apparatus, comprising:

30 a compliant wafer carrier substrate having a first surface and a second surface; and a plurality of chip scale packages, each of the plurality of chip scale packages comprising an integrated circuit die comprising a substrate having a first surface and a second surface, an integrated circuit device, and a plurality of integrated circuit contacts located on the first surface and electrically connected to the integrated circuit device; wherein the second surface of each of the plurality of chip scale packages is adhesively attached to the first surface of the compliant wafer carrier;

35 and wherein each of the plurality of chip scale packages further comprise:

5 a plurality of stress metal springs electrically connected to the integrated circuit contacts, the plurality of stress metal springs comprising a plurality of metal layers, at least two of the metal layers having different initial levels of stress, the stress metal springs defining a loop structure which is rotated by an effective rotation angle away from the first surface of the integrated circuit due to the different initial levels of stress; and

a polymer layer substantially covering the first surface of the integrated circuit and a portion of each of the plurality of stress metal springs, such that a portion of the loop structure of each of the plurality of stress metal springs extends beyond the polymer layer.

10 Support is seen in the Application as filed, at least on page 35, line 26 to page 39, line 22; on page 46, line 32 to page 51, line 18; on page 54, line 15 to page 55, line 13, in Figure 18 to Figure 21; in Figure 55; in Figure 57 to Figure 59; and in Figure 68 to Figure 71.

15 Applicant submits that Claim 22, as amended in independent form, includes all of the limitations of the independent Claim 21, as filed.

20 3b. Applicant has amended Claims 87-89, 91, 92, and 94-96 in independent form, to include all of the limitations of independent Claim 86, as filed. Support is seen in the application as filed, at least on page 36, line 21 to page 39, line 22; on page 46, line 32 to page 51, line 18; on page 54, line 15 to page 55, line 13; in Figure 21; in Figure 55; in Figure 57; in Figure 59; and in Figure 68 to Figure 71.

Applicant has amended Claim 87 to claim a system, comprising:

25 a compliant carrier having a first surface and a second surface;
at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

30 a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

35 wherein the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device are photolithographically patterned springs.

Applicant has amended Claim 88, to claim a system, comprising:

5 a compliant carrier having a first surface and a second surface;

 at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

10 a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

15 a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

20 wherein the plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board are stress metal springs on the upper surface of each of the at least one integrated circuit device.

Applicant has amended Claim 89, to claim a system, comprising:

20 a compliant carrier having a first surface and a second surface;

 at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

25 a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

30 a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

35 wherein each of the plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board are flexible spring probes on the bottom surface of the system board.

Applicant has amended Claim 91, to claim a system, comprising:

35 a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

5 a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface;

 a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board; and

10 a travel limit mechanism which limits perpendicular travel of each of the at least one integrated circuit device in relation to the system board.

Applicant has amended Claim 92, to claim a system, comprising:

15 a compliant carrier having a first surface and a second surface;

 at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

20 a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface;

 a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board; and

25 a pressure plate support;

 wherein the second surface of the compliant carrier is supported on the pressure plate support.

Applicant has amended Claim 94, to claim a system, comprising:

25 a compliant carrier having a first surface and a second surface;

 at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

30 a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;
wherein the compliant carrier is thermally conductive.

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Applicant has amended Claim 95, to claim a system, comprising:

a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at 10 least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

15 a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

wherein the compliant carrier is electrically conductive.

Applicant has amended Claim 96, to claim a system, comprising:

20 a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

25 a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface;

a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

30 at least one interface module having a plurality of electrically conductive pads on a planar region, at least one of the electrically conductive pads connected to at least one interconnection region, and at least one link connected to at least one of the at least one interconnection region; and

35 means for fixedly holding each of the at least one interface module in relation to the system board, such that the plurality of electrically conductive pads on the planar region of

each of the at least one interface module contact at least one of the plurality of electrical conductors on the top surface of the system board.

Applicant submits that Claims 87-89, 91-92, and 94-96, as amended in independent form,
5 include all of the limitations of independent Claim 86, as filed. As Claim 90 depends from
Claim 89, as Claim 93 depends from Claim 92, and as Claims 97-105 depend from Claim
96, and inherently contain all the limitations of the claims they depend from, Claims 90, 93,
and 97-105 inherently include all of the limitations of independent Claim 86, as filed.
Applicant therefore submits that Claims 87-105, as amended, are allowable.

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5. Applicant has amended the Specification, to provide a claim for priority to related
applications.

15 Applicant has also amended the Specification, to provide the correct Patent Number for
U.S. Patent No. 4,758,927 within the "Background of the Invention".

20 Applicant has amended dependent Claim 40, to claim the process of Claim 27, wherein
the sacrificial substrate further comprises at least one groove. Support is seen in the
Application as filed, at least on page 42, line 14 to page 44, line 30; in Claims 40-41; and in
Figure 35 to Figure 39.

25 Applicant has amended dependent Claim 97, to claim the system of Claim 96, wherein
each of the at least one interface module comprises a circuit having a first surface and a
second surface, and wherein the plurality of electrically conductive pads are located on the
first surface. Support is seen in the Application as filed, at least on page 51, line 20 to
page 54, line 13; and in Figure 60 to Figure 67.

30 Applicant has also amended Figure 58, to properly refer to the "columns" with reference
character --339--. Support is seen in the Application as filed, at least on page 50, lines 15-
18; and in Figure 58 and Figure 59.

Applicant has also amended Figure 61, to properly refer to the "dielectric flex circuit
membrane structure" with reference character --342b--. Support is seen in the Application
as filed, at least on page 51 lines 20-30.

6. The Office Action noted that "the references provided by the Applicants have been reviewed and considered". The Office Action also noted that "Applicants must submit PTO-1449 for the Examiner to initial".

5 Applicant has concurrently filed Form PTO-1449, to include cited art disclosed within the background of the Application as filed which was not previously filed on form PTO-1449, and to include other information of which Applicants are aware, which applicants believe may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.25.

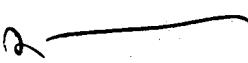
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CONCLUSION

15 Applicant respectfully submits that Claims 23 and 106, as amended, overcome the rejections set forth in the Office Action. Applicant also submits that Claims 22, 87-105, as amended, overcome the objections set forth in the Office Action. Applicant also submits that the amendments do not introduce new matter into the Application. Based on the foregoing, Applicant considers the invention to be in condition for allowance. Applicant earnestly solicits the Examiner's withdrawal of the rejections set forth in the prior Office Action, such that a Notice of Allowance is forwarded to Applicant, and the present 20 application is therefore allowed to issue as a United States patent.

Respectfully Submitted,

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Mark d-up Version to Show Changes in the Specification

Please amend the specification as follows:

5 On page 1, line 3 of the Application as filed, please enter the following section regarding claims for priority:

CLAIM FOR PRIORITY

10 This application claims priority from PCT International Application Number PCT/US01/19792, filed 20 June 2001, which claims priority from U.S. Provisional Application 60/212,923, filed 20 June 2000, and from U.S. Provisional Application 60/213,729, filed 22 June 2000.

15 On page 4, lines 17-33 of the Application as filed, please replace the paragraph with the following paragraph:

W. Berg, *Method of Mounting a Substrate Structure to a Circuit Board*, U.S. Patent No. 4,758,9278 4,758,927 (19 July 1988) discloses "a substrate structure having contact pads 20 is mounted to a circuit board which has pads of conductive material exposed at one main face of the board and has registration features which are in predetermined positions relative to the contact pads of the circuit board. The substrate structure is provided with leads which are electrically connected to the contact pads of the substrate structure and project from the substrate structure in cantilever fashion. A registration element has a plate portion and also 25 has registration features which are distributed about the plate portion and are engageable with the registration features of the circuit board, and when so engaged, maintain the registration element against movement parallel to the general plane of the circuit board. The substrate structure is attached to the plate portion of the registration element so that the leads are in predetermined position relative to the registration features of the circuit board, 30 and in this position of the registration element the leads of the substrate structure overlie the contact pads of the circuit board. A clamp member maintains the leads in electrically conductive pressure contact with the contact pads of the circuit board".

Drawing Am ndm nts

Please amend the Figures as follows:

5 On Figure 58, please replace reference character "139" to --339--, as shown in the replacement formal drawing.

On Figure 61, please replace reference character "142b" to --342b--, as shown in the replacement formal drawing.

Status of the Claims

What is claimed is:

5 1. (Allowed) An apparatus, comprising:

an integrated circuit die comprising a substrate having a first surface and a second surface, and an integrated circuit, and a plurality of integrated circuit contacts located on the first surface and electrically connected to the integrated circuit;

10 contacts, the plurality of stress metal springs comprising a plurality of metal layers at least two of the metal layers having different initial levels of stress, the stress metal springs defining a loop structure which is rotated by an effective rotation angle away from the first surface of the integrated circuit; and

15 a polymer layer substantially covering the first surface of the integrated circuit and a portion of each of the plurality of stress metal springs, such that a portion of the loop structure of each of the plurality of stress metal springs extends beyond the polymer layer.

20 2. (Allowed) The apparatus of Claim 1, wherein the at least two of the metal layers are comprised of the same metal and have an initial stress gradient.

25 3. (Allowed) The apparatus of Claim 1, wherein each of the plurality of stress metal springs further comprises at least one plating layer which substantially covers the loop structure.

30 4. (Allowed) The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises nickel.

5. (Allowed) The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises a nickel alloy.

35 6. (Allowed) The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises gold.

7. (Allowed) The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises silver.

8. (Allowed) The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises rhodium.

9. (Allowed) The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises palladium.

10. (Allowed) The apparatus of Claim 3, wherein at least one of the at least one plating layer comprises cobalt.

10 11. (Allowed) The apparatus of Claim 1, wherein the polymer layer comprises an elastomer.

12. (Allowed) The apparatus of Claim 1, wherein the plurality of integrated circuit contacts comprise contact pads.

15 13. (Allowed) The apparatus of Claim 1, wherein the effective rotation angle is less than 90 degrees.

14. (Allowed) The apparatus of Claim 1, wherein the effective rotation angle is greater than 180 degrees.

20 15. (Allowed) The apparatus of Claim 1, wherein the effective rotation angle is approximately 270 degrees.

25 16. (Allowed) The apparatus of Claim 1, wherein the first metal layer of the plurality of metal layers of each of the plurality of stress metal springs which is directly connected to the integrated circuit and forms the outer convex layer on the loop structure is a boundary layer.

30 17. (Allowed) The apparatus of Claim 1, wherein the boundary layer comprises gold.

18. (Allowed) The apparatus of Claim 1, wherein the boundary layer comprises rhodium.

35 19. (Allowed) The apparatus of Claim 1, wherein the boundary layer comprises palladium.

20. (Allowed) The apparatus of Claim 1, wherein the portion of the loop structure of each of the plurality of stress metal springs which extends beyond the polymer layer further comprises an expanded contact surface.

5 21. (Canceled)

22. (Currently Amended) An apparatus, comprising:

a compliant wafer carrier substrate having a first surface and a second surface; and

a plurality of chip scale packages, each of the plurality of chip scale packages

10 comprising an integrated circuit die comprising a substrate having a first surface and a second surface, an integrated circuit device, and a plurality of integrated circuit contacts located on the first surface and electrically connected to the integrated circuit device;

wherein the second surface of each of the plurality of chip scale packages is adhesively attached to the first surface of the compliant wafer carrier;

15 The apparatus of Claim 21, and wherein each of the plurality of chip scale packages further comprise:

a plurality of stress metal springs electrically connected to the integrated circuit contacts, the plurality of stress metal springs comprising a plurality of metal layers, at least two of the metal layers having different initial levels of stress, the stress metal springs defining a loop structure which is rotated by an effective rotation angle away from the first surface of the integrated circuit due to the different initial levels of stress;; and

a polymer layer substantially covering the first surface of the integrated circuit and a portion of each of the plurality of stress metal springs, such that a portion of the loop structure of each of the plurality of stress metal springs extends beyond the polymer layer.

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23. (Currently Amended). An interposer, comprising:

a an electrically insulative support substrate having a first surface and a second surface; and

5 at least one stress metal spring extending at least from the first surface to the second surface of the support substrate, each of the at least one stress metal spring comprising a plurality of metal layers, at least two of the metal layers having different levels of stress, each of the at least one stress metal spring defining a loop structure which is rotated by an effective rotation angle away from the first surface of the support substrate.

10 24. (Original) The interposer of Claim 23, wherein the support substrate comprises a polymer.

15 25. (Original) The interposer of Claim 23, wherein the support substrate comprises an elastomer.

20 26. (Original) The interposer of Claim 23, wherein the at least two of the metal layers are comprised of the same metal and have an initial stress gradient.

27. (Allowed). A process, comprising the steps of:

20 providing a sacrificial substrate;

establishing a plurality of metal layers on the sacrificial substrate, at least two of the metal layers having different levels of stress;

releasing a portion of the plurality of metal layers to form a non-planar loop structure which is rotated by an effective rotation angle away from the sacrificial substrate;

25 establishing a polymer layer over the sacrificial substrate, the plurality of metal layers, and the formed non-planar loop structure;

removing a portion of the established polymer layer to expose a portion of the formed non-planar loop structure; and

removing the sacrificial substrate.

30 28. (Allowed) The process of Claim 27, wherein the at least two of the metal layers are comprised of the same metal and have an initial stress gradient.

29. (Allowed) The process of Claim 27, wherein the first of the established plurality of
35 metal layers comprises a boundary layer.

30. (Allowed) The process of Claim 29, wherein the boundary layer comprises gold.

31. (Allowed) The process of Claim 29, wherein the boundary layer comprises rhodium.

5 32. (Allowed) The process of Claim 29, wherein the boundary layer comprises palladium.

33. (Allowed) The process of Claim 27, further comprising the step of:
forming at least one plated layer over the non-planar loop structure.

10 34. (Allowed) The process of Claim 33, wherein at least one of the at least one formed
plated layer comprises nickel.

35. (Allowed) The process of Claim 33, wherein at least one of the at least one formed
plated layer comprises a nickel alloy.

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36. (Allowed) The process of Claim 33, wherein at least one of the at least one formed
plated layer comprises gold.

37. (Allowed) The process of Claim 33, wherein at least one of the at least one formed
plated layer comprises rhodium.

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38. (Allowed) The process of Claim 33, wherein at least one of the at least one formed
plated layer comprises palladium.

25 39. (Allowed) The process of Claim 33, wherein at least one of the at least one formed
plated layer comprises cobalt.

40. (Currently Amended) The process of Claim 27, wherein the sacrificial substrate further
comprises ~~a groove~~ at least one groove.

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41. (Allowed) The process of Claim 27, wherein the sacrificial substrate further comprises
a groove, further comprising the step of:
filling the groove with an electrically conductive material;
wherein a portion of the plurality of metal layers is established on the electrically
35 conductive material.

42. (Allowed) The process of Claim 27, wherein the established polymer layer comprises a plurality of polymer layers.

43. (Allowed) The process of Claim 27, wherein the effective rotation angle is less than 90
5 degrees.

44. (Allowed) The process of Claim 27, wherein the effective rotation angle is greater than 180 degrees.

10 45. (Allowed) The process of Claim 27, wherein the effective rotation angle is approximately 270 degrees.

46. (Allowed) A contactor, comprising:

15 a substrate having a first surface and a second surface, and a plurality of conductive vias extending from the first surface to the second surface;

20 a plurality of stress metal springs electrically connected to the vias, the plurality of stress metal springs comprising a plurality of metal layers, at least two of the metal layers having different initial levels of stress, the stress metal springs defining a loop structure which is rotated by an effective rotation angle due to the different initial levels of stress away from the first surface of the substrate, wherein each of the plurality of stress metal springs further comprises a primary plating layer which substantially covers the loop structure.

25 47. (Allowed) The contactor of Claim 46, wherein the primary plating layer comprises nickel.

48. (Allowed) The contactor of Claim 46, wherein the primary plating layer comprises a nickel alloy.

30 49. (Allowed) The contactor of Claim 46, wherein the primary plating layer comprises cobalt.

50. (Allowed) The contactor of Claim 46, further comprising a secondary plating layer over the primary plating layer.

35 51. (Allowed) The contactor of Claim 50, wherein the secondary plating layer comprises rhodium.

52. (Allowed) The contactor of Claim 50, wherein the secondary plating layer comprises gold.

5 53. (Allowed) A contactor, comprising:

a substrate having a first surface and a second surface, and a plurality of conductive vias extending from the first surface to the second surface;

10 a plurality of stress metal springs electrically connected to the vias, the plurality of stress metal springs comprising a plurality of metal layers, at least two of the metal layers having different initial levels of stress, the stress metal springs defining a loop structure which is rotated by an effective rotation angle due to the different initial levels of stress away from the first surface of the substrate; and

15 a polymer layer substantially covering the first surface of the substrate and a portion of each of the plurality of stress metal springs, such that a portion of the loop structure of each of the plurality of stress metal springs extends beyond the polymer layer.

54. (Allowed) The contactor of Claim 53, wherein the at least two of the metal layers are comprised of the same metal and have an initial stress gradient.

20 55. (Allowed) The contactor of Claim 53, wherein each of the plurality of stress metal springs further comprises at least one plating layer which substantially covers the loop structure.

25 56. (Allowed) The contactor of Claim 55, wherein at least one of the at least one plating layer comprises nickel.

57. (Allowed) The contactor of Claim 55, wherein at least one of the at least one plating layer comprises a nickel alloy.

30 58. (Allowed) The contactor of Claim 55, wherein at least one of the at least one plating layer comprises gold.

59. (Allowed) The contactor of Claim 55, wherein at least one of the at least one plating layer comprises rhodium.

60. (Allowed) The contactor of Claim 55, wherein at least one of the at least one plating layer comprises palladium.

61. (Allowed) The contactor of Claim 55, wherein at least one of the at least one plating layer comprises cobalt.

62. (Allowed) The contactor of Claim 53, wherein the polymer layer comprises an elastomer.

10 63. (Allowed) The contactor of Claim 53, wherein the portion of the loop structure of each of the plurality of stress metal springs which extends beyond the polymer layer comprises a contact pad region.

15 64. (Allowed) The contactor of Claim 53, wherein the effective rotation angle is less than 90 degrees.

65. (Allowed) The contactor of Claim 53, wherein the effective rotation angle is greater than 180 degrees.

20 66. (Allowed) The contactor of Claim 53, wherein the effective rotation angle is approximately 270 degrees.

67. (Allowed) A process, comprising the steps of:

providing a contactor substrate having a first surface and a second surface, and a conductive via extending from the first surface to the second surface;

5 establishing a plurality of metal layers on the contactor substrate in electrical contact with the via, at least two of the metal layers having different initial levels of stress;

releasing a portion of the plurality of layers to form a non-planar loop structure which is rotated by an effective rotation angle due to the different initial layers of stress away from the contactor substrate; and

10 forming the support substrate over the contactor substrate and partially over the formed non-planar loop structure.

68. (Allowed) The process of Claim 67, wherein the step of forming the support substrate over the contactor substrate and partially over the formed non-planar loop structure further comprises:

15 establishing the support substrate over the contactor substrate, the plurality of metal layers, and the formed non-planar loop structure; and

removing a portion of the established support substrate to expose a portion of the formed non-planar loop structure.

20 69. (Allowed) The process of Claim 67, wherein effective rotation angle is less than 90 degrees.

70. (Allowed) The process of Claim 67, wherein effective rotation angle is greater than 180 degrees.

25 71. (Allowed) The process of Claim 67, wherein effective rotation angle is approximately 270 degrees.

72. (Allowed) The process of Claim 67, wherein the first of the established plurality of 30 metal layers comprises a boundary layer.

73. (Allowed) The process of Claim 72, wherein the boundary layer comprises gold.

74. (Allowed) The process of Claim 72, wherein the boundary layer comprises rhodium.

35 75. (Allowed) The process of Claim 72, wherein the boundary layer comprises palladium.

76. (Allowed) The process of Claim 67, further comprising the step of:
forming at least one plated layer over the non-planar loop structure.

5 77. (Allowed) The process of Claim 76, wherein at least one of the at least one formed
plated layer comprises nickel.

78. (Allowed) The process of Claim 76, wherein at least one of the at least one formed
plated layer comprises a nickel alloy.

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79. (Allowed) The process of Claim 76, wherein at least one of the at least one formed
plated layer comprises gold.

80. (Allowed) The process of Claim 76, wherein at least one of the at least one formed
15 plated layer comprises rhodium.

81. (Allowed) The process of Claim 76, wherein at least one of the at least one formed
plated layer comprises palladium.

20 82. (Allowed) The process of Claim 76, wherein at least one of the at least one formed
plated layer comprises cobalt.

83. (Allowed) The process of Claim 67, wherein the contactor substrate further comprises
at least one groove.

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84. (Allowed) The process of Claim 67, wherein the contactor substrate further comprises
a groove, further comprising the step of;
filling the groove with an electrically conductive material;
wherein a portion of the plurality of metal layers is established on the electrically
30 conductive material.

85. (Allowed) The process of Claim 67, wherein the established polymer layer comprises
a plurality of polymer layers.

35 86. (Canceled)

87. (Currently Amended) A system comprising:
a compliant carrier having a first surface and a second surface;
at least one integrated circuit device having a lower surface and an upper surface, the
lower surface adhesively attached to the first surface of the compliant carrier, each of the at
5 least one integrated circuit device comprising a plurality of electrical connections on the
upper surface;

10 a system board having a bottom surface and a top surface, and a plurality of
electrical conductors extending between the bottom surface and the top surface; and
10 a plurality of electrically conductive connections between each of the plurality of
electrical connections on the upper surface of each of the at least one integrated circuit
device and each of the electrical conductors on the bottom surface of the system board;

15 The system of Claim 86, wherein the plurality of electrical connections on the upper
surface of each of the at least one integrated circuit device are photolithographically
patterned springs.

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88. (Currently Amended) A system, comprising:

a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

a plurality of electrically conductive connections between each of the plurality of

electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

~~The system of Claim 86, wherein the plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board are stress metal springs on the upper surface of each of the at least one integrated circuit device.~~

89. (Currently Amended) A system, comprising:

a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

~~The system of Claim 86, wherein each of the plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board are flexible spring probes on the bottom surface of the system board.~~

35 90. (Original) The system of Claim 89, wherein the flexible spring probes on the bottom surface of the system board are photolithographically patterned springs.

91. (Currently Amended) A system, comprising:

a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the

lower surface adhesively attached to the first surface of the compliant carrier, each of the at
least one integrated circuit device comprising a plurality of electrical connections on the
upper surface;

a system board having a bottom surface and a top surface, and a plurality of
electrical conductors extending between the bottom surface and the top surface;

a plurality of electrically conductive connections between each of the plurality of
electrical connections on the upper surface of each of the at least one integrated circuit
device and each of the electrical conductors on the bottom surface of the system board; and
The system of Claim 86, further comprising:

a travel limit mechanism which limits perpendicular travel of each of the at least one
integrated circuit device in relation to the system board.

92. (Currently Amended) A system, comprising:

a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the

lower surface adhesively attached to the first surface of the compliant carrier, each of the at
least one integrated circuit device comprising a plurality of electrical connections on the
upper surface;

a system board having a bottom surface and a top surface, and a plurality of
electrical conductors extending between the bottom surface and the top surface;

a plurality of electrically conductive connections between each of the plurality of
electrical connections on the upper surface of each of the at least one integrated circuit
device and each of the electrical conductors on the bottom surface of the system board; and
The system of Claim 86, further comprising:

a pressure plate support;

wherein the second surface of the compliant carrier is supported on the pressure
plate support.

93. (Original) The system of Claim 92, wherein the pressure plate support is compliant.

35 94. (Currently Amended) A system, comprising:

a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

5 a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

10 The system of Claim 86, wherein the compliant carrier is thermally conductive.

95. (Currently Amended) A system, comprising:

a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

15 a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

The system of Claim 86, wherein the compliant carrier is electrically conductive.

96. (Currently Amended) A system, comprising:

a compliant carrier having a first surface and a second surface;

at least one integrated circuit device having a lower surface and an upper surface, the lower surface adhesively attached to the first surface of the compliant carrier, each of the at least one integrated circuit device comprising a plurality of electrical connections on the upper surface;

a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface;

10 a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board;

The system of Claim 86, further comprising:

15 at least one interface module having a plurality of electrically conductive pads on a planar region, at least one of the electrically conductive pads connected to at least one interconnection region, and at least one link connected to at least one of the at least one interconnection region; and

20 means for fixedly holding each of the at least one interface module in relation to the system board, such that the plurality of electrically conductive pads on the planar region of each of the at least one interface module contact at least one of the plurality of electrical conductors on the top surface of the system board.

97. (Currently Amended) The system of Claim 96, wherein each of the at least one interface module includes comprises a circuit having a first surface and a second surface, and wherein the plurality of electrically conductive pads are located on the first surface.

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98. (Original) The system of Claim 97, wherein the circuit is a flexible circuit.

99. (Original) The system of Claim 97, wherein the circuit is a semi-rigid circuit.

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100. (Original) The system of Claim 97, wherein the circuit is a rigid circuit.

101. (Original) The system of Claim 96, further comprising:

at least one buss bar electrically connected to at least one of the at least one interconnection region.

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102. (Original) The system of Claim 101, further comprising:

at least one power control module located on the at least one interface module, each of the at least one power control module electrically connected between the at least one buss bar and at least one of the at least one the interconnection region.

5 103. (Original) The system of Claim 102, wherein the at least one power control module is in thermal contact with the at least one buss bar.

104. (Original) The system of Claim 101, further comprising:

10 at least one power control module located on the at least one buss bar, each of the at least one power control module electrically connected between the at least one buss bar and at least one of the at least one the interconnection region.

105. (Original) The system of Claim 104, wherein the at least one power control module is in thermal contact with the at least one buss bar.

15 106. (Currently Amended) A process, comprising the steps of:

providing a compliant carrier having ~~an~~ a first surface and a second surface;

adhesively attaching a wafer comprising at least one integrated circuit device lower surface and an upper surface on the first surface of the compliant carrier, each of the at least one integrated circuit having a plurality of electrical connections on the upper surface;

separating each of the at least one integrated circuit devices from the other of the at least one integrated circuit devices;

providing a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between the bottom surface and the top surface; and

25 creating a plurality of electrically conductive connections between each of the plurality of electrical connections on the upper surface of each of the at least one integrated circuit device and each of the electrical conductors on the bottom surface of the system board.

107. (Original) The process of Claim 106, further comprising the steps of:

providing at least one interface module having a plurality of electrically conductive pads on a planar region, at least one of the electrically conductive pads connected to at least one interconnection region, and at least one link connected to at least one of the at least one interconnection region; and

fixedly holding each of the at least one interface module in relation to the system board, such that the plurality of electrically conductive pads on the planar region of each of the at least one interface module contact at least one of the plurality of electrical conductors on the top surface of the system board.

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108. (Original) The process of Claim 106, further comprising the step of:

providing a pressure plate support; and
supporting the second surface of the compliant carrier on the pressure plate support.

15 109. (Original) The process of Claim 108, wherein the pressure plate support is compliant.

110. (Original) The process of Claim 106, wherein the compliant carrier is thermally conductive.

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111. (Original) The process of Claim 106, wherein the compliant carrier is electrically conductive.